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| **Batch: B2 Roll No.: 1611103 Experiment / assignment / tutorial No.: 5** |

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| **Title:** Flip Flops |

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**Objective:**Design of JK Flip flop, D flip flop, T flip flop using NAND Gates & verification of the same flip flop using IC7476

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**Expected Outcome of Experiment:**

**CO2:** Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

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**Books/ Journals/ Websites referred:**

* R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill
* M .Morris Mano, “Digital Logic & computer Design”, PHI
* A.P.Godse, D.A.Godse, “Digital Logic Design”

**Pre Lab/ Prior Concepts:**

Flip-flop is the common name given to two-state devices which offer basic memory for sequential logic operations. Flip-flops are heavily used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data.

**JK-flip flop:** has two inputs, traditionally labeled J and K. IC 7476 is a dual JK master slave flip flop with preset and clear inputs. If J and K are different then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock edge, then the output will toggle from one state to the other. It can perform the functions of the set/reset flip-flop and has the advantage that there are no ambiguous states.

**D Flip Flop:** tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. D flip-flop can be made from J-K flip-flop by connecting both inputs through a not gate.

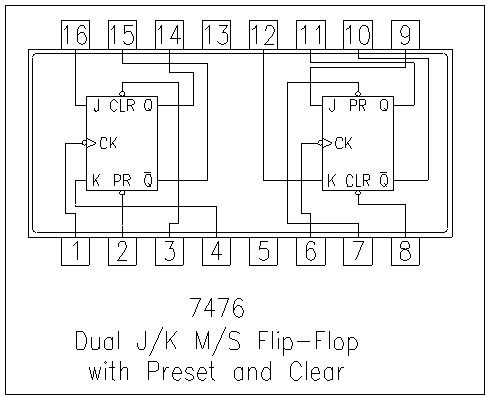
**T Flip Flop:** T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

**Implementation Details:**

**Procedure**

1. Locate IC 7476 on Digital trainer kit
2. Apply various inputs to J & K pins by means of the output on logic output indicator.
3. Connect a pulsar switch to the clock input.
4. Connect the J&K as D and T flip flop as shown in diagrams and verify the respective truth tables.

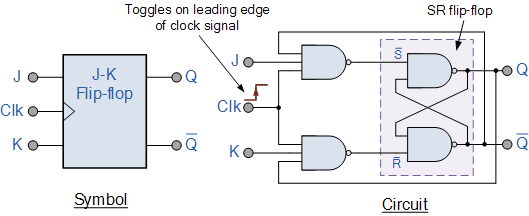
**Pin Diagram of IC 7476 JK Master- Slave FF**



**Logic Symbol Truth Table**

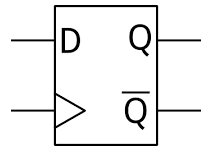
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **J** | **K** | **Q** | **Q’** | **Qn+1** | **Qn+1’**  **n+1** |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | **1** |

**JKFF**

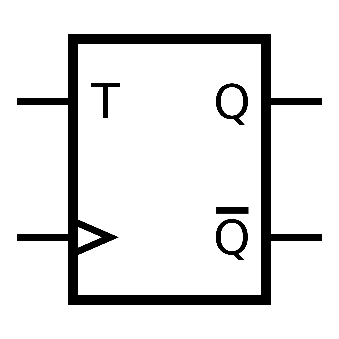


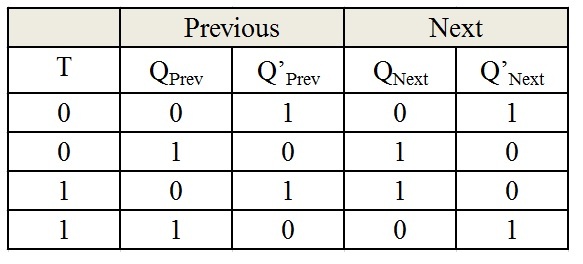
**D FF Truth Table**

|  |  |
| --- | --- |
| **D** | **O/P** |
| 0 | 0 |
| 1 | 1 |

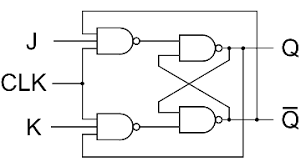


**TFF Truth Table**





**Diagram of JK Flip Flop using NAND gates**



**Conclusion:**

Hence design of JK Flip flop, D flip flop, T flip flop using NAND Gates & verification of the same flip flop using IC7476 is implemented.

**Post Lab Descriptive Questions**

1. How does a JK flip-flop differ from an SR flip-flop in its basic operation?
2. What is use of characteristic and excitation table?
3. How many flip flops due you require storing the data 1101?
4. Describe the basic difference between pulse-triggered and edge-triggered flip-flops.

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1 JK flip flop is made up of SR flip flop. On high inputs JK toggles the previous values whereas SR enters “*Race*” state. When S is low the output is “*Set”* and when R is low the output is cleared that is “0”. In JK Flip Flop the output is according to J input except for the cases when both inputs are same. In JK Flip Flop there is a clock, preset and clear option as well. No such thing exists in SR flip flop.

2 In [electronics design](https://en.wikipedia.org/wiki/Electronics_design), an **excitation table** shows the minimum inputs that are necessary to generate a particular next state (in other words, to **"excite"** it to the next state) when the current state is known. They are similar to [truth tables](https://en.wikipedia.org/wiki/Truth_table) and [state tables](https://en.wikipedia.org/wiki/State_table), but rearrange the data so that the current state and next state are next to each other on the left-hand side of the table, and the inputs needed to make that state change happen are shown on the right side of the table. In order to obtain the excitation table of a [flip-flop](https://en.wikipedia.org/wiki/Flip-flop_(electronics)), one needs to draw the Q(t) and Q(t+1) for all possible cases (e.g., 00,01,10 and 11), and then make the value of flip-flop such that on giving this value, one shall receive the input as Q(t+1) as desired.

3 Since the number is 4 bits long we will require 4 JK flip flops to store 1101.

4 A pulse can be generated by moving a switch from Low to High then back to Low. So the pulse-triggered FF needs a complete pulse Low -High - Low. And edge triggered can be divided into two:  
Positive edge triggered ---> Low to High transition.  
Negative edge triggered ---> High to Low transition.